NASA TECH BRIEF

Multiple-Mask Chemical Etching

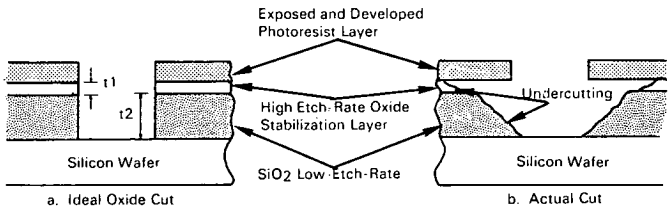

Fig. 1. Standard Semiconductor Photoetching Process

Fig. 2. Multiple Masking, Technique 1

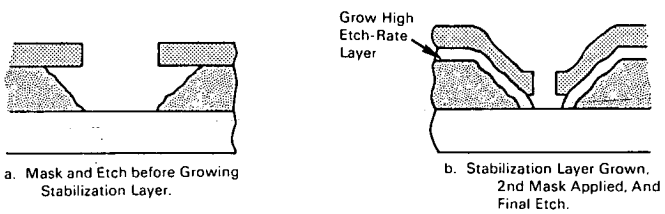

Fig. 3. Multiple Masking, Technique 2

The problem:

Standard chemical etching techniques, which remove semiconductor oxides during the fabrication of integrated circuits, sometimes result in excessive lateral etching. An ideal etched profile is shown in Figure 1; however, in practice, the etchant removes a larger area at the top. If a high etch-rate oxide (t_1) is located in the structure, an area will be etched laterally for a distance equal to many oxide thicknesses resulting in the exposure of critical areas of the device.

The solution:

The lateral etching has been contained by using multiple masking techniques which effectively reduce the total area of the high etch-rate oxide exposed to the chemical etchant.

How it's done:

One method utilizes a short-term etch which removes only the high etch-rate top layer from the silicon oxide surface. The etchant is neutralized and a second

(continued overleaf)

mask is applied as shown in Figure 2. A second etch is then initiated to cut through the slow etch-rate silicon oxide layer (t_2). The second mask preserves the high etch-rate stabilization layer and reduces lateral undercutting because of the reduced opening size (m_2) of the second mask.

A second technique, multiple contacts, consists of first masking and etching before the high etch-rate stabilizing oxide layer is grown. Figure 3a shows the first photoresist mask and resulting etch; the first mask is removed and the top oxide then grown. A second photoresist mask with slightly smaller openings is then applied to the surface and a second etching follows. As shown in Figure 3b, the stabilizing high etch-rate oxide layer and the original opening are protected from the etchant; the total lateral etch is now less than $t_1 + t_2$.

Note:

No further documentation is available. Inquiries may be directed to:

Technology Utilization Officer
Manned Spacecraft Center
Houston, Texas 77058
Reference: B69-10221

Patent status:

No patent action is contemplated by NASA.

Source: Don Lee Cannon of
Lockheed Electronics Company
under contract to
Manned Spacecraft Center
(MSC-13114)